3A, 24V, 340KHz Synchronous Step-Down Converter

DESCRIPTION

The EUP3484S is a synchronous current mode buck regulator capable of driving 3A continuous load current with excellent line and load regulation. The EUP3484S can operate with an input range 4.5V to 24V and the output can be externally set from 0.925V to 18V with a resistor divider.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. In shutdown mode the regulator draws 1μA of supply current. Programmable soft-start minimizes the inrush supply current and the output overshoot at initial startup. Automatic pulse skipping mode operation increase efficiency at light loads.

The EUP3484S require a minimum number of external components.

FEATURES

- 3A Output Current
- Automatic Pulse Skipping Mode at Light Load
- Integrated 160mΩ/110mΩ DMOS Switches
- 4.5V to 24V Input Operating Range
- Output Adjustable from 0.925V to 18V
- Up to 95% Efficiency
- 1μA Shutdown Current
- Fixed 340KHz Frequency
- Programmable Soft-Start
- Thermal Shutdown and Overcurrent Protection
- Input Supply Undervoltage Lockout
- 230ns Minimum On Time
- Available in SOP-8 (EP) Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- PC Monitors
- Portable Electronics

Typical Application Circuit

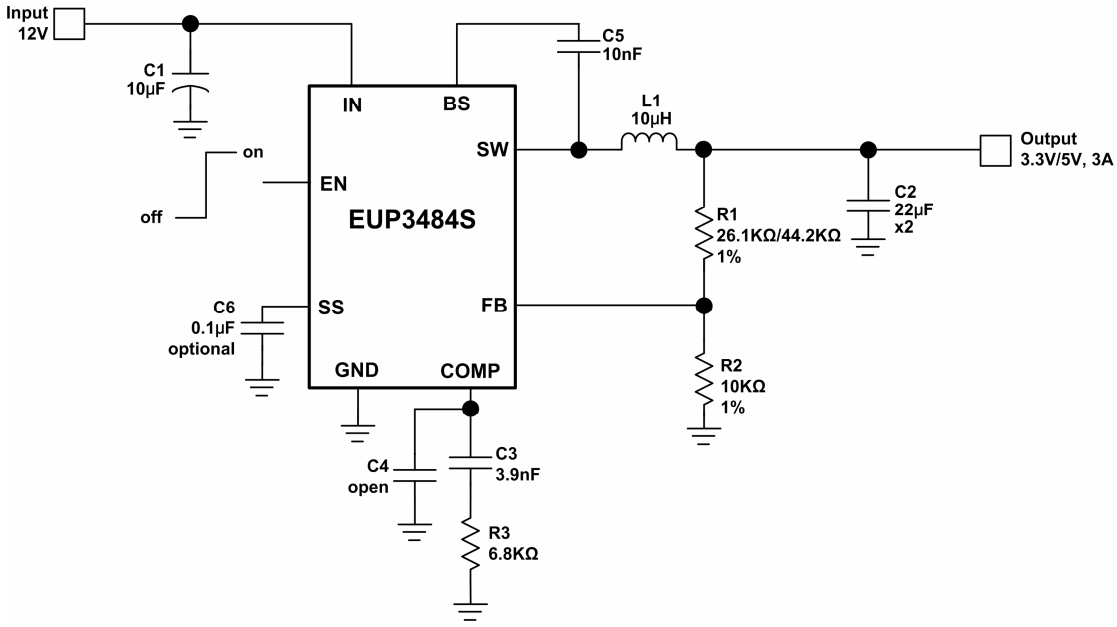
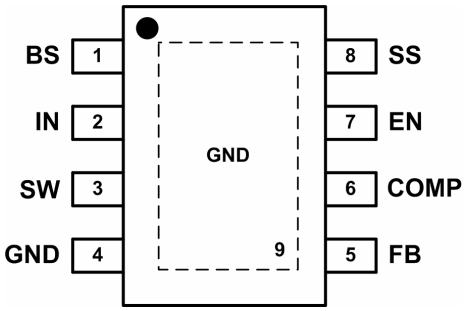


Figure 1. 12V to 3.3V/5V Application Circuit

Pin Configurations

Package Type	Pin Configurations
SOP-8 (EP)	

Pin Description

PIN	PIN NAME	DESCRIPTION
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel DMOS switch. Connect a 0.01µF or greater capacitor from SW to BS to power the high side switch.
2	IN	Input Supply Pin. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.5V to 24V power source. Bypass IN to GND with a suitably large capacitor to minimize input ripple to the IC. See ***Input Capacitor Section of the applications notes.***
3	SW	Power Switching Output. Connect the output LC filter from SW to the output load.
4 9 (Exposed Pad)	GND	Ground. GND pin should be connected to the exposed thermal pad for proper operation. This power thermal pad should be connected to PCB ground plane using multiple vias for good thermal performance.
5	FB	Output Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage. The feedback threshold is 0.925V. ***See Setting the Output Voltage***.
6	COMP	Loop compensation Input. Connect a series RC network from COMP to GND to compensate the regulation control loop. ***See Compensation.***
7	EN	Enable Input. EN is a logic input that controls the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Don't leave EN pin floating. Directly connect EN to IN (or through a resistance) for automatic startup.
8	SS	Soft-Start Control Input. Connect an external capacitor to program the soft-start. If unused, leave it open, which means internal soft-start function.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP3484SDIR1	SOP-8 (EP)	xxxxx 3484S	-40 °C to +85°C

EUP3484S □ □ □ □

Lead Free Code
1: Lead Free, Halogen-Free

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
D: SOP

Block Diagram

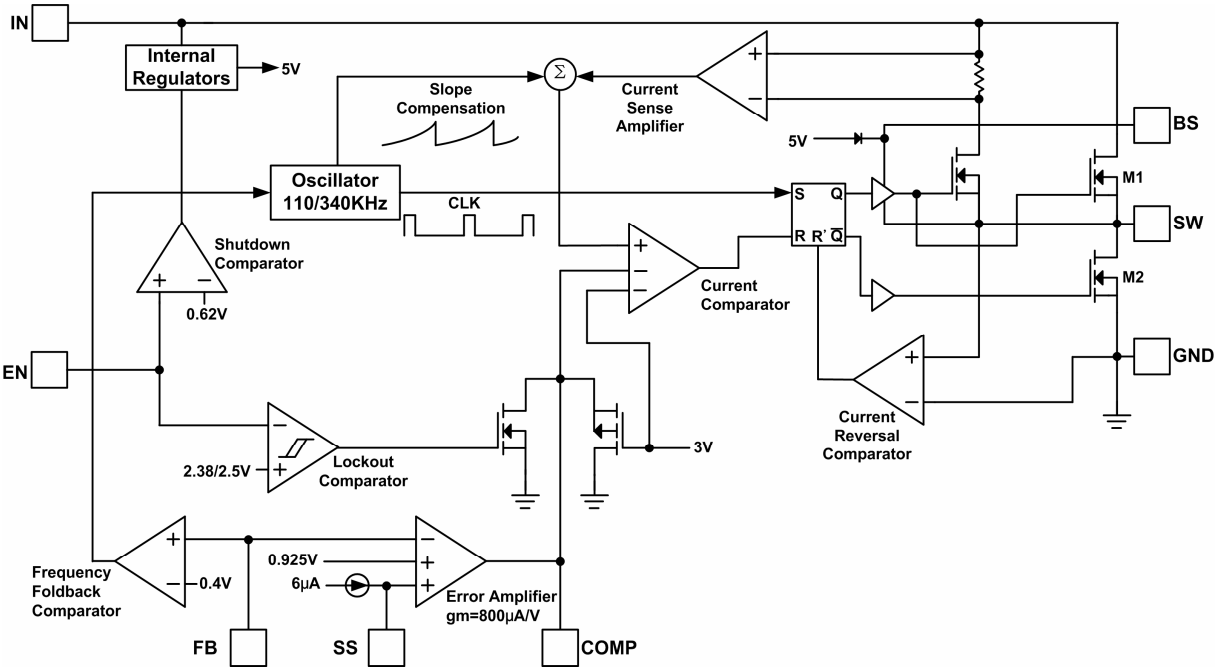


Figure 2.Functional Block Diagram

Absolute Maximum Ratings (1)

- Supply Voltage (V_{IN}) ---------- -0.3V to +28V
- Enable Voltage (V_{EN}) ---------- -0.3V to +28V
- Switch Voltages (V_{SW}) ---------- -1V to V_{IN} +0.3V
- Boot Voltage (V_{BS}) ---------- V_{SW} -0.3V to V_{SW} +6V
- All Other Pins ---------- -0.3V to +6V
- Junction Temperature ---------- 150°C
- Lead Temperature ---------- 260°C
- Storage Temperature ---------- -65°C to +150°C
- Output Voltage V_{OUT} ---------- 0.925V to 18V
- Thermal Resistance θ_{JA} (SOP-8_EP) ---------- 60°C /W
- Thermal Resistance θ_{JC} (SOP-8_EP) ---------- 20°C /W
- Maximum Power Dissipation (P_D) ---------- 2.083W

Recommend Operating Conditions (2)

- Input Voltage V_{IN} ---------- 4.5V to 24V
- Ambient Operating Temp ---------- -40°C to +85°C

Note(1):Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note(2):The device is not guaranteed to function outside the recommended operating conditions.

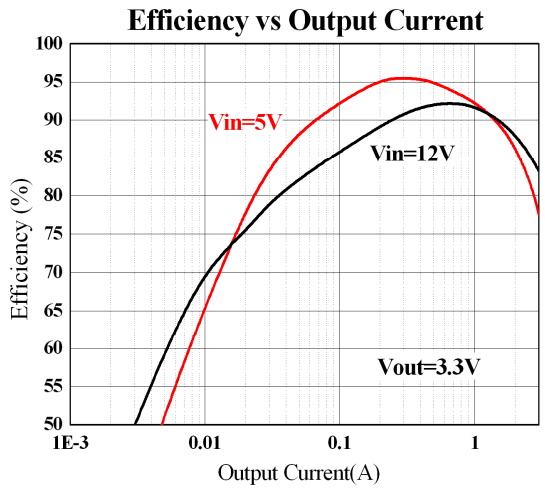
Electrical Characteristics

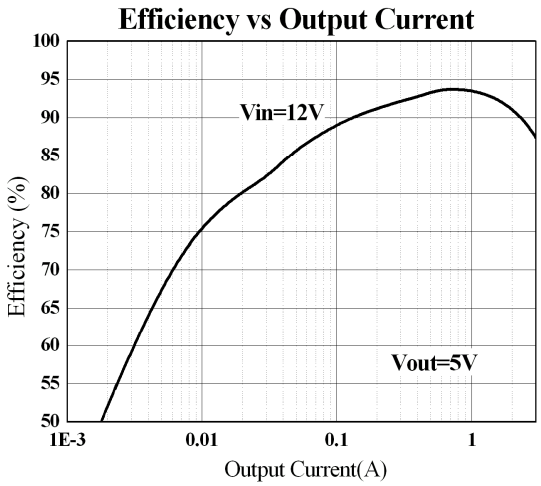
The ● denote specifications which apply over the full operating temperature range, otherwise specification are VIN=12V , T_A=25°C unless otherwise specified.

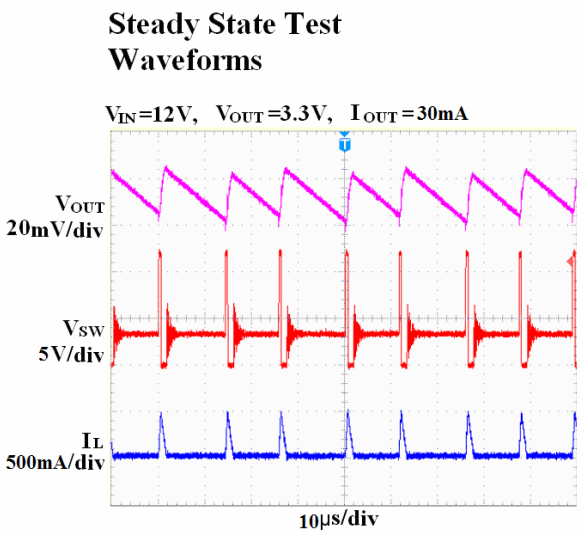
Parameter	Conditions		EUP3484S			Unit
			Min	Typ	Max.	
Shutdown Supply Current	V_{EN}=0V			1	5	μA
Supply Current	V_{FB}=1V			0.45	0.9	mA
Feedback Voltage	4.5≤ V_{IN} ≤24V		0.907	0.925	0.943	V
		●	0.897	0.925	0.953	
Error Amplifier Voltage Gain				360		V/V
Error Amplifier Transconductance	ΔI_C = ±10μA			800		μA/V
High-Side Switch On-Resistance				160		mΩ
Low-Side Switch On-Resistance				110		mΩ
High-Side Switch Leakage Current	V_{EN}=0V, V_{SW}=0V				5	μA
Upper Switch Current Limit	Minimum Duty Cycle		3.8	5.5		A
Lower Switch Current Limit	From Drain to Source			0		A
COMP to Current Sense Transconductance				7.5		A/V
Oscillation Frequency			300	340	380	KHz
Short Circuit Oscillation Frequency	V_{FB}=0V			110		KHz
Maximum Duty Cycle	V_{FB}=0.7V			90		%
Minimum On Time				230		ns
EN Disable Threshold		●	0.36	1.5	2.0	V
EN Lockout Threshold	V_{EN} Rising		2.3	2.5	2.8	V
		●	2	2.5	3	
EN Lockout Threshold Hysteresis				210		mV
Input Under Voltage Lockout Threshold	V_{IN} Rising		3.8	4.1	4.4	V
Soft-Start Charge Current	V_{SS}=0V			6		μA
Thermal Shutdown				160		°C

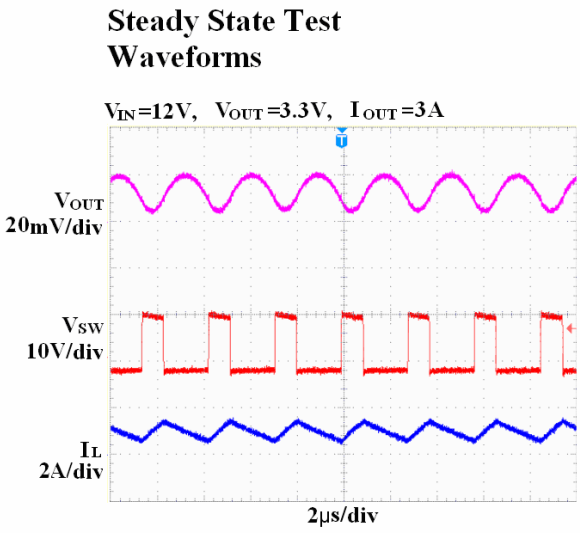
Typical Operating Characteristics

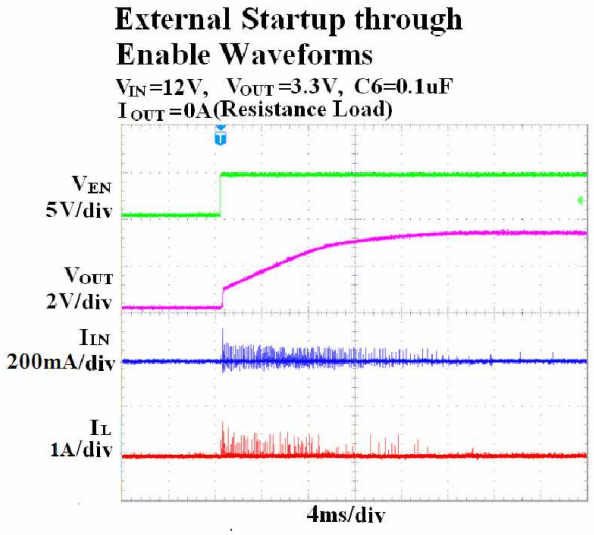
(See Figure1, C1 =10μF, C2=22μF× 2, L=10μH, T_A=+25°C)

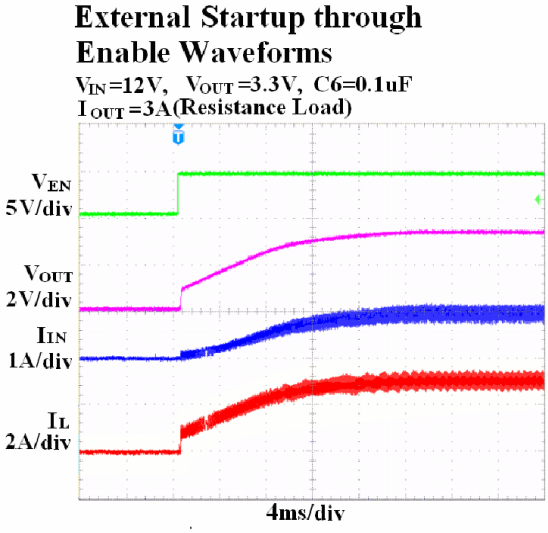










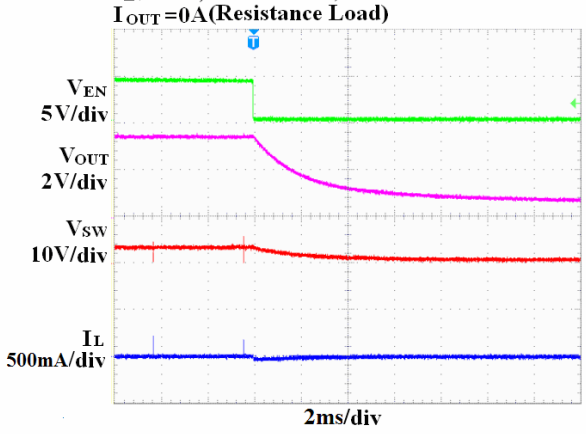


Typical Operating Characteristics (continued)

(See Figure1, C1 =10µF, C2=22µF× 2, L=10µH, T_A=+25°C)

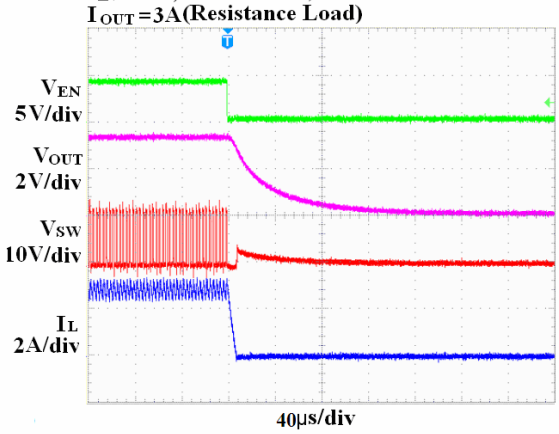
Shutdown through Enable Waveforms

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A(Resistance Load)



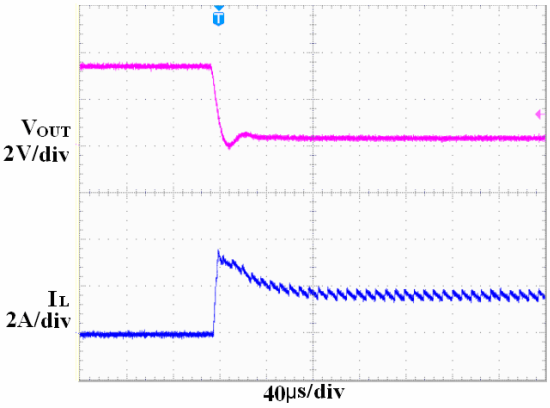
Shutdown through Enable Waveforms

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A(Resistance Load)



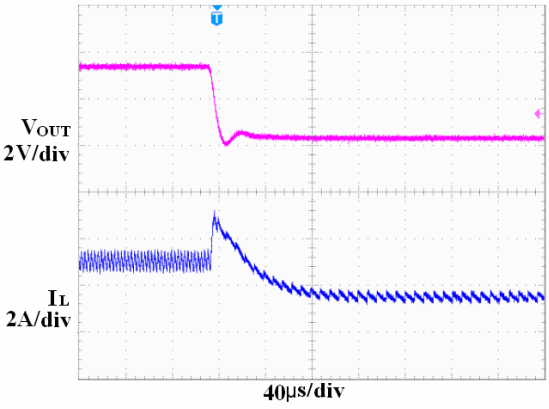
Short Circuit Test Waveforms

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A



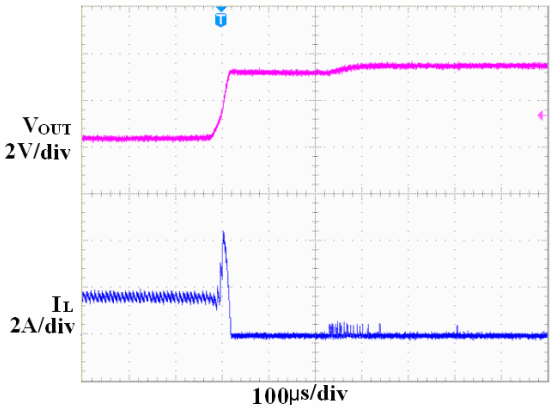
Short Circuit Test Waveforms

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A



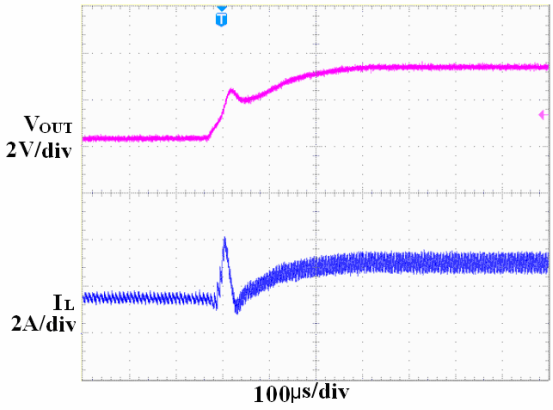
Short Circuit Recovery Waveforms

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A



Short Circuit Recovery Waveforms

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A

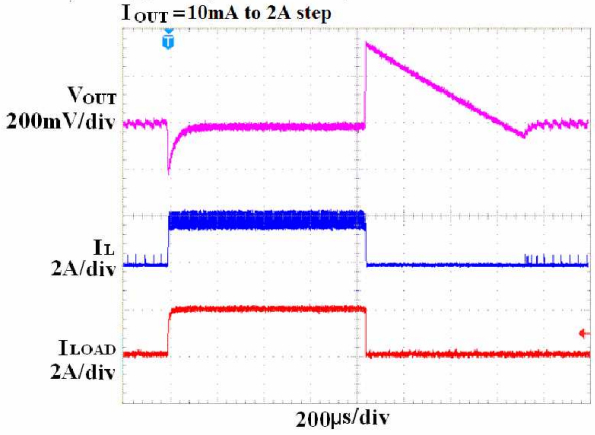


Typical Operating Characteristics (continued)

(See Figure1, C1 =10µF, C2=22µF× 2, L=10µH, T_A=+25°C)

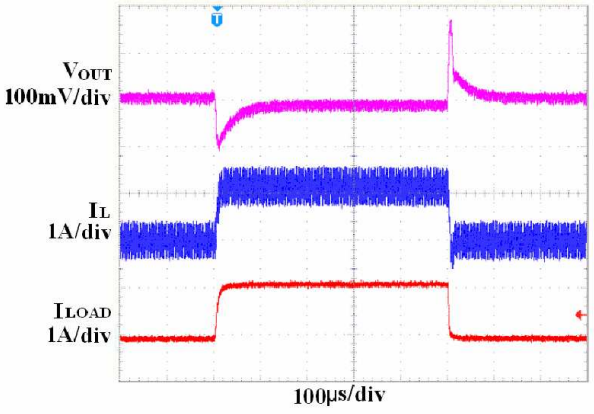
Load Transient Test Waveforms

V_{IN}=12V, V_{OUT}=3.3V,
I_{OUT}=10mA to 2A step



Load Transient Test Waveforms

V_{IN}=12V, V_{OUT}=3.3V,
I_{OUT}=1A to 2A step



Functional Description

The EUP3484S regulates input voltages from 4.5V to 24V down to an output voltage as low as 0.925V, and supplies up to 3A of load current.

The EUP3484S uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at the COMP pin is compared to the switch current (measured internally) to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

At light loads, the inductor current may reach zero or reverse on each pulse. The bottom DMOS is turned off by the current reversal comparator and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator. At light load, the EUP3484S will automatically skip pulses in pulse skipping mode operation to maintain output regulation and increases efficiency.

When the FB pin voltage exceeds 15% of the nominal regulation value of 0.925V, the over voltage comparator is tripped and forcing the high-side switch off.

Application Information

Setting the Output Voltage

The output voltage is set using a resistive voltage divider connected from the output voltage to FB. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1 + R2}$$

Thus the output voltage is:

$$V_{OUT} = 0.925 * \frac{R1 + R2}{R2}$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using the typical value for R2, R1 is determined by:

$$R1 = 10.81 * \left(V_{OUT} - 0.925\right) (k\Omega)$$

For example, for a 3.3V output voltage, R2 is 10kΩ and R1 is 26.1kΩ.

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit.

The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 * f_S * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Optional Schottky Diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode may be high and cause efficiency loss. An optional small 1A Schottky diode B130 in parallel with low-side switch is recommended to improve overall efficiency when input voltage is higher.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C1 * f_S} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C1 is the input capacitance value.

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * \left(R_{ESR} + \frac{1}{8 * f_S * C2}\right)$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 * f_S^2 * L * C2} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The EUP3484S can be optimized for a wide range of capacitance and ESR values.

Compensation Components

EUP3484S employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to govern the characteristics of the control system.
The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} * G_{CS} * A_{VEA} * \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage (0.925V), A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi * C3 * A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi * C2 * R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi * C3 * R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi * C2 * R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C4) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi * C4 * R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback

loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause the system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used:

1. Choose the compensation resistor (R3) to set the desired crossover frequency.

Determine R3 by the following equation:

$$R3 = \frac{2\pi * C2 * f_C}{G_{EA} * G_{CS}} * \frac{V_{OUT}}{V_{FB}}$$

$$< \frac{2\pi * C2 * 0.1 * f_S}{G_{EA} * G_{CS}} * \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency, which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (f_{Z1}) below one-forth of the crossover frequency provides sufficient phase margin.

Determine C3 by the following equation:

$$C3 > \frac{4}{2\pi * R3 * f_C}$$

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C4) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi * C2 * R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C4) to set the pole f_{P3} at the location of the ESR zero. Determine C4 by the equation:

$$C4 = \frac{C2 * R_{ESR}}{R3}$$

To simplify design efforts using the EUP3484S，the typical design for common application are listed in Table1.

External Bootstrap Diode

It is recommended that an external bootstrap diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator.

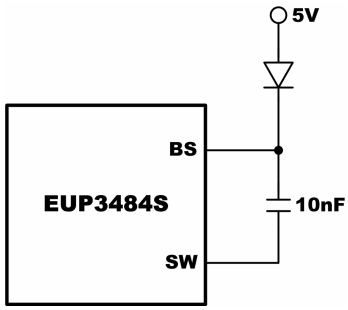


Figure 3. Add Optional External Bootstrap Diode to Enhance

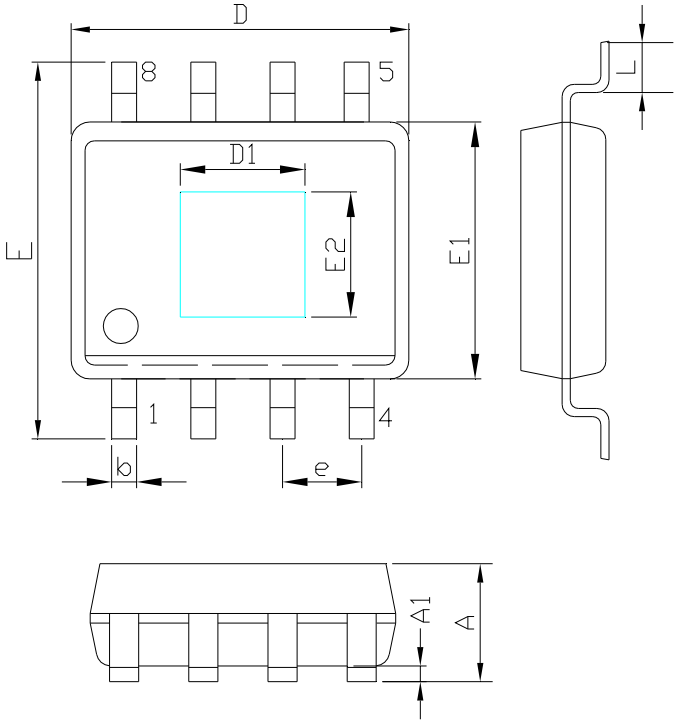
This diode is also recommended for high duty cycle operation (when $\frac{V_{OUT}}{V_{IN}}$ >65%) and high output voltage (V_{OUT} >12V) applications.

Table1. External Components for Typical Designs

Vin(V)	Vout(V)	L1(μH)	C2(μF)	R1(KΩ)	R2(KΩ)	R3(KΩ)	C3(nF)	C4(pF)
5	1.0	3.3	22*2	0.820	10	6.8	3.9	open
5	1.2	4.7	22*2	3.0	10	6.8	3.9	open
5	3.3	10	22*2	26.1	10	6.8	3.9	open
12	1.0	3.3	22*2	0.820	10	2.2	10	open
12	1.2	4.7	22*2	3.0	10	2.2	10	open
12	3.3	10	22*2	26.1	10	6.8	3.9	open
12	5.0	10	22*2	44.2	10	6.8	3.9	open

Packaging Information

SOP-8 (EP)



Remark: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	1.35	-	1.75	0.053	-	0.069
A1	0.00	-	0.25	0.000	-	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.70	3.90	4.00	0.146	0.154	0.157
D1	2.67	2.97	3.50	0.105	0.117	0.138
E2	1.78	2.18	2.60	0.070	0.086	0.102
E	5.80	6.00	6.20	0.228	0.236	0.244
L	0.40	-	1.27	0.016	-	0.050
b	0.31	-	0.51	0.012	-	0.020
e	1.27			0.050		