## Protection IC for 1-Cell Battery Pack

## Features

- High Detection Accuracy
- Overcharge Detection: $\pm 25 \mathrm{mV}$
- Overdischarge Detection: $\pm 50 \mathrm{mV}$
- Discharge Overcurrent Detection: $\pm 15 \mathrm{mV}$
- Charge Overcurrent Detection: $\pm 30 \mathrm{mV}$
- High Withstand Voltage
- Absolute maximum ratings: 28 V
(V- pin and CO pin)
- Ultra Small Package
- SOT-23-5
- SOT-23-6
- DFN-6L


## Application

- Mobile phone battery packs

■ Digital camera battery packs

- Bluetooth earphone Li-ion battery module


## Description

The NT1702 series are the 1-cell protection IC for lithium-ion/lithium-polymer rechargeable battery pack. The high accuracy voltage detector and delay time circuits are built in NT1702 series with state-of-art design and process.
To minimize power consumption, NT1702 series activates power down mode when an overdischarge event is detected (for power-down mode enabled version). Besides, NT1702 series performs protection functions with four external components for miniaturized PCB .

The tiny package is especially suitable for compact portable device, i.e. slim mobile phone and Bluetooth earphone.

## Typical Application Circuit



## Package and Pin Description

NT1702A description
SOT-23-5


| Pin No. | Symbol | NT1702A pin description |
| :---: | :---: | :--- |
| 1 | V- | Voltage detection between V- pin and Vss pin <br> (Overcurrent / charger detection pin) |
| 2 | VDD | Connection for positive power supply input |
| 3 | Vss | Connection for negative power supply input |
| 4 | DO | Connection of discharge control FET gate |
| 5 | CO | Connection of charge control FET gate |

SOT-23-6


| Pin No. | Symbol | NT1702A pin description |
| :---: | :---: | :--- |
| 1 | DO | Connection of discharge control FET gate |
| 2 | V- | Voltage detection between V- pin and VSS pin <br> (Overcurrent / charger detection pin) |
| 3 | CO | Connection of charge control FET gate |
| 4 | NC | No connection |
| 5 | VDD | Connection for positive power supply input |
| 6 | Vss | Connection for negative power supply input |

DFN-6L


| Pin No. | Symbol | NT1702A pin description |
| :---: | :---: | :--- |
| 1 | NC | No connection |
| 2 | CO | Connection of charge control FET gate |
| 3 | DO | Connection of discharge control FET gate |
| 4 | Vss | Connection for negative power supply input |
| 5 | VDD | Connection for positive power supply input |
| 6 | V- | Voltage detection between V- pin and VSS pin <br> (Overcurrent / charger detection pin) |

## Ordering Information

NT1702A-XXX XX
Package Type
A5: SOT-23-5
A6: SOT-23-6
B3: DFN-6L
Version code
Serial number: A

## Product version code:

(1) SOT-23-6

Table1: (For Li-ion or Li-polymer battery cell)

| NT1702 | Overcharge <br> Detection Voltage $V_{\text {DET1 }}(\mathrm{V})$ | Over charge Release Function | Overcharge <br> Release <br> Voltage <br> $V_{\text {REL1 }}(\mathrm{V})$ | Over discharge Detection Voltage $V_{\text {DET2 }}(V)$ | Over discharge Release Voltage $V_{\text {REL2 }}(V)$ | Overcurrent <br> Detection Voltage $V_{\text {DET3 }}(\mathrm{V})$ | OV Battery <br> Charge <br> Function | Power down mode Function | Delay time |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| HFK | 4.280 | (b) | 4.130 | 2.800 | 3.100 | 0.150 | Unavailable | Yes | (1) |
| HQM | 4.280 | (b) | 4.080 | 2.300 | 2.300 | 0.130 | Unavailable | Yes | (1) |
| HQR | 4.280 | (b) | 4.080 | 2.300 | 2.300 | 0.100 | Unavailable | Yes | (1) |
| HFR | 4.280 | (b) | 4.130 | 2.800 | 3.100 | 0.100 | Unavailable | Yes | (1) |
| FLK | 4.325 | (a) | 4.125 | 2.500 | 2.900 | 0.150 | Unavailable | Yes | (1) |
| GZK | 4.300 | (b) | 4.100 | 2.500 | 2.900 | 0.150 | Unavailable | Yes | (1) |
| JQM | 4.275 | (a) | 4.075 | 2.300 | 2.300 | 0.130 | Available | Yes | (2) |

(2) SOT-23-5

Table 2: (For Li-ion or Li-polymer battery cell)

| NT1702 | Overcharge <br> Detection Voltage $V_{\text {DET1 }}(\mathrm{V})$ | Over charge Release Function | Overcharge <br> Release <br> Voltage <br> $V_{\text {REL1 }}(\mathrm{V})$ | Over discharge Detection Voltage $V_{\text {DET2 }}(\mathrm{V})$ | Over discharge Release Voltage $V_{\text {REL2 }}(\mathrm{V})$ | Overcurrent <br> Detection <br> Voltage <br> $V_{\text {DET3 }}(\mathrm{V})$ | OV Battery Charge Function | Power down mode Function | Delay time |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| HFK | 4.280 | (b) | 4.130 | 2.800 | 3.100 | 0.150 | Unavailable | Yes | (1) |
| HQR | 4.280 | (b) | 4.080 | 2.300 | 2.300 | 0.100 | Unavailable | Yes | (1) |
| HFR | 4.280 | (b) | 4.130 | 2.800 | 3.100 | 0.100 | Unavailable | Yes | (1) |
| HXW | 4.280 | (b) | 4.280 | 2.800 | 2.800 | 0.050 | Unavailable | Yes | (1) |
| JQM | 4.275 | (a) | 4.075 | 2.300 | 2.300 | 0.130 | Available | Yes | (2) |

(3) DFN-6L

Table 3: (For Li-ion or Li-polymer battery cell)

| NT1702 | Overcharge <br> Detection <br> Voltage <br> $V_{\text {DET1 }}(\mathrm{V})$ | Over <br> charge <br> Release <br> Function | Overcharge <br> Release <br> Voltage <br> $V_{\text {REL1 }}(\mathrm{V})$ | Over <br> discharge <br> Detection <br> Voltage <br> $\mathrm{V}_{\text {DET2 }}(\mathrm{V})$ | Over <br> discharge <br> Release <br> Voltage <br> $\mathrm{V}_{\text {REL2 }}(\mathrm{V})$ | Overcurrent <br> Detection <br> Voltage <br> $V_{\text {DET3 }}(\mathrm{V})$ | OV Battery <br> Charge <br> Function | Power <br> down <br> mode <br> Function | Delay <br> time |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| HFK | 4.280 | (b) | 4.130 | 2.800 | 3.100 | 0.150 | Unavailable | Yes | $(1)$ |
| HQM | 4.280 | (b) | 4.080 | 2.300 | 2.300 | 0.130 | Unavailable | Yes | $(1)$ |
| HQR | 4.280 | (b) | 4.080 | 2.300 | 2.300 | 0.100 | Unavailable | Yes | $(1)$ |
| HFR | 4.280 | (b) | 4.130 | 2.800 | 3.100 | 0.100 | Unavailable | Yes | $(1)$ |
| FLK | 4.325 | (a) | 4.125 | 2.500 | 2.900 | 0.150 | Unavailable | Yes | $(1)$ |
| HXW | 4.280 | (b) | 4.280 | 2.800 | 2.800 | 0.050 | Unavailable | Yes | $(1)$ |
| JQM | 4.275 | (a) | 4.075 | 2.300 | 2.300 | 0.130 | Available | Yes | $(2)$ |

Remark

1. Please contact our sales office for the products with detection voltage value other than those specified above.
2. Please reference the session "Overcharge Protection Release" for more detail about overcharge release function (a) and (b)
3. Please reference the characteristics for delay time, (1) and (2)

Table4: (For Detection Delay Time)

| Delay time | Overcharge delay <br> time <br> $\mathrm{t}_{\text {DET } 1}(\mathrm{~S})$ | Overdischarge <br> delay time <br> $\mathrm{t}_{\text {DET2 }}(\mathrm{mS})$ | Discharge <br> overcurrent delay <br> time <br> $\mathrm{t}_{\text {DET } 3}(\mathrm{mS})$ | Charge overcurrent <br> delay time <br> $\mathrm{t}_{\text {DET } 4}(\mathrm{mS})$ | Load <br> short-circuiting <br> delay time <br> $\mathrm{t}_{\text {SHORT }}(\mathrm{uS})$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $(1)$ | 1.2 | 150 | 9 | 9 | 300 |
| $(2)$ | 1.2 | 38 | 9 | 9 | 300 |

Absolute Maximum Ratings

| Symbol | Descriptions |  | Rating | Units |
| :---: | :---: | :---: | :---: | :---: |
| $V_{\text {DD }}$ | Supply Voltage |  | -0.3 to 7 | V |
| $V$ - | V-pin |  | $\mathrm{V}_{\mathrm{DD}}-28$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| $\mathrm{V}_{\mathrm{co}}$ | Output Voltage | CO pin | $\mathrm{V}_{\mathrm{DD}}-28$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| $V_{\text {D }}$ |  | DO pin | Vss -0.3 to $\mathrm{V}_{\text {DD }}+0.3$ | V |
| $\mathrm{P}_{\mathrm{D}}$ | Power Dissipation | $\begin{gathered} \hline \text { SOT-23-5 \& } \\ \text { SOT23-6 } \\ \hline \end{gathered}$ | 250 | mW |
|  |  | DFN-6L | 250 |  |
| T ${ }_{\text {OPT }}$ | Operating Temperature Range |  | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\text {STG }}$ | Storage Temperature Range |  | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |

Applying any over "Absolute Maximum Ratings" practice can permanently damage the device. These data are indicated the absolute maximum values only but not implied any operating performance.

## Electrical Characteristics

$\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right)$

| Symbol | Item | Conditions | MIN | TYP | MAX | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Detection Voltage |  |  |  |  |  |  |
| $V_{\text {DET1 }}$ | Overcharge detection voltage | -- | $V_{\text {det } 1-0.025 ~}^{\text {a }}$ | $V_{\text {DET1 }}$ | $V_{\text {DET } 1}+0.025$ | V |
| $\mathrm{V}_{\text {ReL1 }}$ | Overcharge release voltage | $\mathrm{V}_{\mathrm{DET} 1} \neq \mathrm{V}_{\text {REL1 }}$ | $\mathrm{V}_{\text {REL } 100.05}$ | $V_{\text {REL1 }}$ | $\mathrm{V}_{\text {REL } 1}+0.05$ | V |
|  |  | $V_{\text {DET } 1}=\mathrm{V}_{\text {REL } 1}$ | $V_{\text {REL } 1-0.025 ~}^{\text {a }}$ | $V_{\text {REL } 1}$ | $\mathrm{V}_{\text {REL } 1}+0.025$ | V |
| $\mathrm{V}_{\text {DET2 }}$ | Over-discharge detection voltage | -- | $V_{\text {DET2-0.05 }}$ | $V_{\text {DET2 }}$ | $\mathrm{V}_{\text {DET2 }}+0.05$ | V |
| $V_{\text {ReL2 }}$ | Over-discharge release voltage | $\mathrm{V}_{\text {DET2 }} \neq \mathrm{V}_{\text {REL2 }}$ | $V_{\text {Rel2-0.10 }}$ | $V_{\text {REL2 }}$ | $V_{\text {REL2 }}+0.10$ | V |
|  |  | $V_{\text {DET2 }}=V_{\text {REL2 }}$ | $V_{\text {Rel2 }}$-0.05 | $V_{\text {REL2 }}$ | $\mathrm{V}_{\text {REL2 }}+0.05$ | V |
| $V_{\text {DET3 }}$ | Discharge overcurrent detection voltage | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | $V_{\text {DET3-0.015 }}$ | $V_{\text {DET }}$ | $\mathrm{V}_{\text {DET }}+0.015$ | V |
| $V_{\text {DET4 }}$ | Charge overcurrent detection | $V_{D D}=3.5 \mathrm{~V}$ | -0.13 | -0.10 | -0.07 | V |
| $V_{\text {Short }}$ | Load short-circuiting detection voltage | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | 0.30 | 0.50 | 0.70 | V |

Current Consumption (power-down function enabled)

| $V_{D D}$ | Operating input voltage | $V_{D D}-V_{S S}$ | 2.2 |  | 6.0 |
| :---: | :--- | :---: | :---: | :---: | :---: |
| $I_{D D}$ | Supply current | $V_{D D}=3.5 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}$ | 1.0 | 3.0 | 5.5 |
| $I_{\text {STANDBY }}$ | Power-down current (power-down <br> function enabled IC only) | $V_{D D}=2.0 \mathrm{~V}, \mathrm{~V}-$ floating |  | $\mu \mathrm{V}$ |  |

OV battery Charging Function

| $V_{\text {OCHA }}$ | $0 ~ V$ battery charge starting charger <br> voltage | 0 V battery charging <br> function "available" | 0.5 | 1.0 | 1.5 | V |
| :---: | :--- | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {OINH }}$ | OV battery charge inhibition battery <br> voltage | 0 V battery charging <br> function "unavailable" <br> (Vcharger=4V~14V) | 0.2 | 0.3 | 1.5 | V |


| Symbol | Item | Conditions | MIN | TYP | MAX | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Resistance |  |  |  |  |  |  |
| $\mathrm{R}_{\text {COH }}$ | CO pin H resistance | $\begin{gathered} \mathrm{V}_{\mathrm{CO}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \\ \mathrm{~V}-=0 \mathrm{~V} \end{gathered}$ | - | 5 | 10 | K $\Omega$ |
| R col | CO pin L resistance | $\begin{gathered} \mathrm{V}_{\mathrm{CO}}=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=4.5 \mathrm{~V}, \\ \mathrm{~V}-=0 \mathrm{~V} \end{gathered}$ | - | 5 | 10 | M ת |
| R ${ }_{\text {DOH }}$ | DO pin H resistance | $\begin{gathered} \mathrm{V}_{\mathrm{DO}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \\ \mathrm{~V}-=0 \mathrm{~V} \end{gathered}$ | - | 5 | 10 | K $\Omega$ |
| RDOL | DO pin L resistance | $\begin{gathered} \mathrm{VDO}=0.5 \mathrm{~V}, \mathrm{VDD}=1.8 \mathrm{~V}, \\ \mathrm{~V}-=0 \mathrm{~V} \end{gathered}$ | - | 5 | 10 | K $\Omega$ |

## V- internal Resistance

| $\mathrm{R}_{\text {VMD }}$ | Internal resistance between V - and <br> $\mathrm{V}_{\mathrm{DD}}$ | $\mathrm{V}_{\mathrm{DD}}=1.8 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}$ | 100 | 300 | 900 | $\mathrm{~K} \Omega$ |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\mathrm{Vмs}}$ | Internal resistance between V - and <br> $\mathrm{V}_{\mathrm{SS}}$ | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \mathrm{~V}-=1.0 \mathrm{~V}$ | 100 | 200 | 400 | $\mathrm{~K} \Omega$ |

Electrical Characteristics
$\left(\mathrm{Ta}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}\right)^{*}$
Symbol
Item

| Conditions | MIN |
| :--- | :--- |

TYP
MAX $\quad$ Unit

Detection Voltage

| $V_{\text {DET1 }}$ | Overcharge detection voltage | -- | $\mathrm{V}_{\text {DET } 1}-0.060$ | $\mathrm{V}_{\text {DET1 }}$ | $\mathrm{V}_{\mathrm{DET} 1}+0.040$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {REL1 }}$ | Overcharge release voltage | $\mathrm{V}_{\mathrm{DET} 1} \neq \mathrm{V}_{\text {REL } 1}$ | $V_{\text {REL } 1-0.08 ~}^{\text {a }}$ | $V_{\text {REL1 }}$ | $V_{\text {REL } 1+0.065 ~}^{\text {a }}$ | V |
|  |  | $\mathrm{V}_{\mathrm{DET} 1}=\mathrm{V}_{\text {REL } 1}$ | $\mathrm{V}_{\text {REL } 1-0.060 ~}^{\text {a }}$ | $V_{\text {REL1 }}$ | $V_{\text {REL } 1+0.040 ~}^{\text {a }}$ | V |
| $V_{\text {DET2 }}$ | Over-discharge detection voltage | -- | $V_{\text {DET2-0.11 }}$ | $V_{\text {det2 }}$ | $\mathrm{V}_{\text {DET2 }}+0.13$ | V |
| $V_{\text {REL2 }}$ | Over-discharge release voltage | $\mathrm{V}_{\mathrm{DET} 2} \neq \mathrm{V}_{\text {REL2 }}$ | $\mathrm{V}_{\text {REL2 } 2} 0.15$ | $V_{\text {REL2 }}$ | $\mathrm{V}_{\text {REL2 }}+0.19$ | V |
|  |  | $V_{\text {DET2 }}=\mathrm{V}_{\text {REL2 }}$ | $\mathrm{V}_{\text {REL2 }}-0.11$ | $V_{\text {REL2 }}$ | $\mathrm{V}_{\text {REL2 }}+0.13$ | V |
| $V_{\text {DET3 }}$ | Discharge overcurrent detection voltage | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | $\mathrm{V}_{\text {DET }}$-0.021 | $V_{\text {det3 }}$ | $\mathrm{V}_{\mathrm{DET} 3}+0.024$ | V |
| $V_{\text {DET4 }}$ | Charge overcurrent detection | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | -0.14 | -0.10 | -0.06 | V |
| $V_{\text {SHORT }}$ | Load short-circuiting detection voltage | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | 0.16 | 0.50 | 0.84 | V |

Current Consumption (power-down function enabled)

| $V_{D D}$ | Operating input voltage | $V_{D D}-V_{S S}$ | 2.2 |  | 6.0 | V |
| :---: | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{DD}}$ | Supply current | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}$ |  | 3.0 | 7.0 | $\mu \mathrm{~A}$ |
| $\mathrm{I}_{\mathrm{STANDBY}}$ | Power-down current (power-down <br> function enabled IC only) | $\mathrm{V}_{\mathrm{DD}}=2.0 \mathrm{~V}, \mathrm{~V}$ - floating |  |  | 0.3 | $\mu \mathrm{~A}$ |

OV battery Charging Function

| $V_{\text {OCHA }}$ | 0 V battery charge starting charger <br> Voltage | 0 V battery charging <br> function "available" | 0.3 | 1.0 | 1.7 | V |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\text {OINH }}$ | OV battery charge inhibition battery <br> voltage | 0 V battery charging <br> function "unavailable" <br> (Vcharger=4V~14V) | 0.1 | 0.3 | 1.7 | V |

Output Resistance

| $R_{\text {COH }}$ | CO pin H resistance | $V_{C O}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.5 \mathrm{~V}$, <br> $\mathrm{V}=0 \mathrm{~V}$ | - | 5 | 15 | $\mathrm{~K} \Omega$ |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\mathrm{COL}}$ | CO pin L resistance | $\mathrm{V}_{\mathrm{CO}}=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=4.5 \mathrm{~V}$, <br> $\mathrm{V}=0 \mathrm{~V}$ | - | 5 | 15 | $\mathrm{M} \Omega$ |
| $\mathrm{R}_{\mathrm{DOH}}$ | DO pin H resistance | $\mathrm{V}_{\mathrm{DO}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.5 \mathrm{~V}$, <br> $\mathrm{V}=0 \mathrm{~V}$ | - | 5 | 15 | $\mathrm{~K} \Omega$ |
| $\mathrm{R}_{\mathrm{DOL}}$ | DO pin L resistance | $\mathrm{V}_{\mathrm{DO}}=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=1.8 \mathrm{~V}$, <br> $\mathrm{V}=0 \mathrm{~V}$ | - | 5 | 15 | $\mathrm{~K} \Omega$ |

V- internal Resistance

| $R_{\text {VMD }}$ | Internal resistance between V - and <br> $\mathrm{V}_{\mathrm{DD}}$ | $\mathrm{V}_{\mathrm{DD}}=1.8 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}$ | 78 | 300 | 1310 | $\mathrm{~K} \Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\mathrm{VMS}}$ | Internal resistance between V - and <br> $\mathrm{V}_{S S}$ | $\mathrm{~V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \mathrm{~V}-=1.0 \mathrm{~V}$ | 72 | 200 | 440 | $\mathrm{~K} \Omega$ |

*: The specification for this temperature range is guaranteed by design because products are not screened at high to low temperature.

Detection Delay time (1)

| Symbol | Item | Conditions | MIN | TYP | MAX | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Delay Time ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ ) |  |  |  |  |  |  |
| tvdet1* | Output delay time of overcharge | - | 0.96 | 1.2 | 1.4 | s |
|  |  | $\begin{gathered} V_{\mathrm{DD}}=4.28 \mathrm{~V}, \mathrm{C}_{\mathrm{ISS}}=1200 \mathrm{pF}, \\ \mathrm{~V}_{\mathrm{TH}}=0.6 \mathrm{~V} \end{gathered}$ | 0.96 | 1.22 | 1.42 | s |
|  |  | $\begin{gathered} V_{\mathrm{DD}}=4.28 \mathrm{~V}, \mathrm{C}_{\mathrm{ISS}}=1200 \mathrm{pF}, \\ \mathrm{~V}_{\mathrm{TH}}=0.4 \mathrm{~V} \end{gathered}$ | 0.95 | 1.23 | 1.43 | s |
| tvdet2 | Output delay time of overdischarge | $\mathrm{V}_{\text {DET2 }}>2.5 \mathrm{~V}$ | 120 | 150 | 180 | ms |
|  |  | $\mathrm{V}_{\text {DET2 }} \leqq 2.5 \mathrm{~V}$ | 100 | 150 | 200 | ms |
| tvdet3 | Output delay time of discharge over current | $V_{D D}=3.5 \mathrm{~V}$ | 7.2 | 9 | 11 | ms |
|  |  | $\mathrm{V}_{\text {DET2 }} \leqq 2.5 \mathrm{~V}$ | 6 | 9 | 12 | ms |
| $\mathrm{t}_{\text {SHORT }}$ | Output delay time of Load short-circuiting detection | $V_{D D}=3.5 \mathrm{~V}$ | 240 | 300 | 360 | $\mu \mathrm{S}$ |
| tvdet4* | Output delay time of charge over current | $V_{D D}=3.5 \mathrm{~V}$ | 7.2 | 9 | 11 | ms |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \\ & \mathrm{C}_{I S S}=1200 \mathrm{pF}, \mathrm{~V}_{T H}=0.6 \mathrm{~V} \end{aligned}$ | 15.1 | 19.5 | 23.8 | ms |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \\ & \mathrm{C}_{\mathrm{ISS}}=1200 \mathrm{pF}, \mathrm{~V}_{\mathrm{TH}}=0.4 \mathrm{~V} \end{aligned}$ | 16.8 | 21.6 | 26.4 | ms |

Delay Time ( $\mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ )

| tvdet1 | Output delay time of overcharge | - | 0.7 | 1.2 | 2.0 | s |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {vdet2 }}$ | Output delay time of overdischarge | $\mathrm{V}_{\text {DET2 }}>2.5 \mathrm{~V}$ | 83 | 150 | 255 | ms |
|  |  | $\mathrm{V}_{\text {DET } 2} \leqq 2.5 \mathrm{~V}$ | 64 | 150 | 275 | ms |
| tvdet3 | Output delay time of discharge over current | $V_{D D}=3.5 \mathrm{~V}$ | 5 | 9 | 15 | ms |
|  |  | $\mathrm{V}_{\text {DET2 }} \leqq 2.5 \mathrm{~V}$ | 3.8 | 9 | 16 | ms |
| $\mathrm{t}_{\text {SHORT }}$ | Output delay time of Load short-circuiting detection | $V_{D D}=3.5 \mathrm{~V}$ | 150 | 300 | 540 | $\mu \mathrm{S}$ |
| tvdet4 | Output delay time of charge over current | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | 5 | 9 | 15 | ms |

*: Please note that a N-channel MOSFET "turning off delay time" will be affected by 1.Input capacitance ( $\mathrm{C}_{\mathrm{ISs}}$ ). 2.Gate threshold voltage ( $\mathrm{V}_{\mathrm{TH}}$ ); It causes the delay times of overcharge ( $\mathrm{t} \mathrm{V}_{\mathrm{DET} 1}$ ) and charge overcurrent ( $\mathrm{t} \mathrm{V}_{\mathrm{DET4} 4}$ ) of NT 1702 are prolonged approximately " 10 ms " to turn off the N -channel MOSFETs to cutting off the current flowing path.

Detection Delay time (2)

| Symbol | Item | Conditions | MIN | TYP | MAX | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Delay Time ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ ) |  |  |  |  |  |  |
| tvdet1* | Output delay time of overcharge | - | 0.96 | 1.2 | 1.4 | s |
|  |  | $\begin{gathered} \mathrm{V}_{\mathrm{DD}}=4.28 \mathrm{~V}, \mathrm{C}_{\mathrm{ISS}}=1200 \mathrm{pF}, \\ \mathrm{~V}_{\mathrm{TH}}=0.6 \mathrm{~V} \end{gathered}$ | 0.96 | 1.22 | 1.42 | s |
|  |  | $\begin{gathered} V_{D D}=4.28 \mathrm{~V}, C_{\text {ISS }}=1200 \mathrm{pF}, \\ V_{T H}=0.4 \mathrm{~V} \end{gathered}$ | 0.95 | 1.23 | 1.43 | s |
| tvdet2 | Output delay time of overdischarge | $\mathrm{V}_{\text {DET2 }}>2.5 \mathrm{~V}$ | 30 | 38 | 46 | ms |
|  |  | $\mathrm{V}_{\text {DET2 }} \leqq 2.5 \mathrm{~V}$ | 25 | 38 | 51 | ms |
| tvdet3 | Output delay time of discharge over current | $V_{D D}=3.5 \mathrm{~V}$ | 7.2 | 9 | 11 | ms |
|  |  | $\mathrm{V}_{\text {DET2 }} \leqq 2.5 \mathrm{~V}$ | 6 | 9 | 12 | ms |
| tshort | Output delay time of Load short-circuiting detection | $V_{D D}=3.5 \mathrm{~V}$ | 240 | 300 | 360 | $\mu \mathrm{S}$ |
| tvDET4* | Output delay time of charge over current | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | 7.2 | 9 | 11 | ms |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \\ & \mathrm{C}_{\mathrm{ISS}}=1200 \mathrm{pF}, \mathrm{~V}_{T H}=0.6 \mathrm{~V} \end{aligned}$ | 15.1 | 19.5 | 23.8 | ms |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}, \\ & \mathrm{C}_{I S S}=1200 \mathrm{pF}, \mathrm{~V}_{\mathrm{TH}}=0.4 \mathrm{~V} \end{aligned}$ | 16.8 | 21.6 | 26.4 | ms |

Delay Time ( $\mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ )

| tvdet1 | Output delay time of overcharge | - | 0.7 | 1.2 | 2.0 | s |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {vdet }}$ | Output delay time of overdischarge | $\mathrm{V}_{\text {DET } 2}>2.5 \mathrm{~V}$ | 21 | 38 | 65 | ms |
|  |  | $V_{\text {DET2 }} \leqq 2.5 \mathrm{~V}$ | 16 | 38 | 70 | ms |
| tvdet | Output delay time of discharge over current | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | 5 | 9 | 15 | ms |
|  |  | $\mathrm{V}_{\text {DET2 }} \leqq 2.5 \mathrm{~V}$ | 3.8 | 9 | 16 | ms |
| $\mathrm{t}_{\text {SHORT }}$ | Output delay time of Load short-circuiting detection | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | 150 | 300 | 540 | $\mu \mathrm{S}$ |
| tvdet 4 | Output delay time of charge over current | $\mathrm{V}_{\mathrm{DD}}=3.5 \mathrm{~V}$ | 5 | 9 | 15 | ms |

*: Please note that a N-channel MOSFET "turning off delay time" will be affected by 1.Input capacitance ( $\mathrm{C}_{I S S}$ ). 2.Gate threshold voltage ( $\mathrm{V}_{\mathrm{TH}}$ ); It causes the delay times of overcharge ( $\mathrm{t} \mathrm{V}_{\mathrm{DET} 1}$ ) and charge overcurrent ( $\mathrm{t} \mathrm{V}_{\mathrm{DET}}$ ) of NT 1702 are prolonged approximately " 10 ms " to turn off the N -channel MOSFETs to cutting off the current flowing path.

## Test Circuits

■ Overcharge, overdischarge and the release detection voltages (test circuit 1)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$, then NT1702 series enters operating mode.
2) Increase V 1 voltage (from 3.5 V ) gradually. The V 1 voltage is the overcharge detection voltage ( $\mathrm{V}_{\mathrm{DET} 1}$ ) when CO pin goes low (from high).
3) Decrease V 1 gradually. The V 1 voltage is the overcharge release detection voltage $\left(\mathrm{V}_{\mathrm{REL}}\right)$ when CO pin goes high again.
4) Continue decreasing V 1 . The V 1 voltage is the overdischarge detection voltage $\left(\mathrm{V}_{\mathrm{DET} 2}\right)$ when DO pin goes low. Then increase V1 gradually. The V1 voltage is the overdischarge release detection voltage ( $\mathrm{V}_{\text {REL2 }}$ ), when DO pin returns to high.
Note: The overcharge and overdischarge release voltages are defined in versions.

- Discharge overcurrent detection voltage (test circuit 1)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$ and NT 1702 series enters operating condition.
2) Increase V 2 (from 0 V ) gradually. The V 2 voltage is the discharge overcurrent detection voltage ( $\mathrm{V}_{\mathrm{DET}}$ ) when DO pin goes low (from high).

■ Charge overcurrent detection voltage (test circuit 1)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 3=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{OFF}$ and $\mathrm{S} 2=\mathrm{ON}$ and NT 1702 series enters operating condition.
2) Increase V 3 gradually. The V 3 voltage is the charge overcurrent detection voltage $\left(\mathrm{V}_{\mathrm{DET4}}\right)$ when CO pin goes low (from high).

- Load short-circuiting detection voltage (test circuit 1)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$ and NT 1702 series enters operating condition.
2) Increase V2 immediately (within 10uS) till DO pin goes "low" from high with a delay time which is between the minimum and the maximum of Load short-circuiting delay time.

■ Overcharge, overdischarge delay time (test circuit 1)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$ to enter operating condition.
2) Increase V 1 from $\mathrm{V}_{\mathrm{DET} 1}-0.2 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{DET} 1}+0.2 \mathrm{~V}$ immediately (within 10us). The overcharge detection delay time ( $\mathrm{t}_{\mathrm{VDET} 1}$ ) is the period from the time V 1 gets to $\mathrm{V}_{\mathrm{DET1}}+0.2 \mathrm{~V}$ till CO pin switches from high to low.
3) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$ to enter operating condition.
4) Decrease V 1 from $\mathrm{V}_{\mathrm{DET} 2}+0.2 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{DET2}}-0.2 \mathrm{~V}$ immediately (within 10us). The overdischarge detection delay time ( $\mathrm{t}_{\mathrm{VDET} 2}$ ) is the period from the time V 1 gets to $\mathrm{V}_{\text {DET2 }}-0.2 \mathrm{~V}$ till DO pin switches from high to low.

■ Discharge overcurrent delay time (test circuit 1)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$ to enter operating condition.
2) Increase V 2 from 0 V to 0.25 V immediately (within 10us). The discharge overcurrent detection delay time ( $\mathrm{t}_{\mathrm{VDET}}$ ) is the period from the time V 2 gets to 0.25 V till DO pin switches from high to low.

- Charge overcurrent delay time (test circuit 1)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 3=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{OFF}$ and $\mathrm{S} 2=\mathrm{ON}$ to enter operating condition.
2) Increase V 3 from 0 V to 0.3 V immediately (within 10us). The charge overcurrent detection delay time ( $\mathrm{t}_{\text {VDET4 }}$ ) is the period from the time V 3 gets to 0.3 V till CO pin gets to low from high.

■ Load short-circuiting delay time (test circuit 1)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$ to enter operating condition.
2) Increase V 2 from 0 V to 1.0 V immediately (within 10 us ). The Load short-circuiting detection voltage delay time ( $\mathrm{t}_{\text {SHORT }}$ ) is the period from the time V 2 gets to 1.0 V till DO pin switches from high to low.

■ Operating \& power down current consumption (test circuit 2)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}$ and $\mathrm{S} 1=\mathrm{ON}$ to enter operating condition and measure the current I . 11 is the operating condition current consumption (IDD).
2) Set $\mathrm{V} 1=\mathrm{V} 2=2.0 \mathrm{~V}$ and $\mathrm{S} 1=\mathrm{ON}$ enter overdischarge condition and measure current I . 11 is the power down current consumption (I $\mathrm{I}_{\text {standby }}$ ).

■ Resistance between V- and Vdd, V- and Vss (test circuit 2)

1) Set $\mathrm{V} 1=1.8 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}$ and $\mathrm{S} 1=\mathrm{ON}$ and NT 1702 series enters overdischarge condition. $\mathrm{V} 1 / \mathrm{I} 2$ is the internal resistance between V - and VDD pin ( $\mathrm{R}_{\mathrm{Vмд}}$ ).
2) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=1.0 \mathrm{~V}$ and $\mathrm{S} 1=\mathrm{ON}$ and NT 1702 series enters discharge overcurrent condition. $\mathrm{V} 2 / \mathrm{I} 2$ is the internal resistance between V - and Vss pin ( $\mathrm{R}_{\mathrm{vмs}}$ ).

- Output resistance (test circuit 3)

1) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~V} 3=3.0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{OFF}$ and $\mathrm{S} 2=\mathrm{ON}$ to enter operating condition. $(\mathrm{V} 3-\mathrm{V} 1) / 12$ is the internal resistance ( $\mathrm{R}_{\mathrm{COH}}$ ).
2) Set $\mathrm{V} 1=4.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~V} 3=0.5 \mathrm{~V}, \mathrm{~S} 1=\mathrm{OFF}$ and $\mathrm{S} 2=\mathrm{ON}$ to enter overcharge condition. $\mathrm{V} 3 / \mathrm{I} 2$ is the internal resistance ( $R_{\text {Col }}$ ).
3) Set $\mathrm{V} 1=3.5 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~V} 3=3.0 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$ to enter operating condition. $(\mathrm{V} 3-\mathrm{V} 1) / 12$ is the internal resistance $\left(\mathrm{R}_{\mathrm{DOH}}\right)$.
4) Set $\mathrm{V} 1=1.8 \mathrm{~V}, \mathrm{~V} 2=0 \mathrm{~V}, \mathrm{~V} 3=0.5 \mathrm{~V}, \mathrm{~S} 1=\mathrm{ON}$ and $\mathrm{S} 2=\mathrm{OFF}$ to enter overdischarge condition. $\mathrm{V} 3 / \mathrm{I} 2$ is the internal resistance ( $\mathrm{R}_{\mathrm{DOL}}$ ).

- OV battery charge starting charger voltage (products with OV battery charging function is "Available") (test circuit 4)

1) Set $\mathrm{V} 1=\mathrm{V} 2=0 \mathrm{~V}$, decrease V 2 gradually.
2) The V 2 voltage is the 0 V charge starting voltage $\left(\mathrm{V}_{\text {ОСнА }}\right)$ when CO pin switches from low to high $\left(\mathrm{V}_{\mathrm{V}_{-}}+\right.$ 0.1 V or higher).

- OV battery charge inhibition battery voltage (products with OV battery charging function is
"Unavailable") (test circuit 4)

1) Set $\mathrm{V} 1=0 \mathrm{~V}$, $\mathrm{V} 2=-4 \mathrm{~V}$ and increase V 1 gradually.
2) The V 1 voltage is the 0 V charge inhibition voltage $\left(\mathrm{V}_{\text {oinh }}\right)$ when CO pin switches from low to high $\left(\mathrm{V}_{\mathrm{V}_{-}+}\right.$ 0.1 V or higher).

Note: The charger voltage should not be higher than 14 V of 0 V battery charge inhibition battery voltage.

## Recommended:

1) ' 0 V charge available' doesn't means NT1702 can recover the zero-V cell to be full charged if this cell has been already damaged due to too low voltage.
2) In NT1702, the ' 0 V charge inhibition' voltage is rather lower ( $0.3 \mathrm{~V} \sim 0.5 \mathrm{~V}$ ). That is, NT1702 allows charging such low voltage cell and recover it.
3) For safety consideration, we strongly recommended to select ' 0 V charge inhibition' to prevent from charging a damaged cell.

## Test Circuit



Test circuit 1


Test circuit 3


Test circuit 2


Test circuit 4

## Operation

The NT1702 series provides overcharge, overdischarge, discharge overcurrent, charge overcurrent and load short-circuiting protections for the 1-cell battery pack. NT1702 series continuously monitors the voltage of battery between VDD pin and VSS pin to control overcharge and overdischarge protections. When the battery pack is in charging stage, the current flows from the charger to the battery through EB+ and EB-; the voltage between Vpin and VSS pin is negative. On the other hand, when the battery pack is in discharging stage, the current flows from battery to the load through EB+ and EB-; the voltage between V- pin and VSS pin is positive. The NT1702 series also monitors the voltage which is determined by the current of charge and discharge and the series Rds(on) of MOSFETs between V- pin and Vss pin to detect charge overcurrent and discharge overcurrent current conditions.

## (1) Normal Condition (Operation mode)

The NT1702 series turns both the charging and discharging control MOSFETs on when the voltage of battery is in the range from overcharge detection voltage $\left(\mathrm{V}_{\mathrm{DET1}}\right)$ to overdischarge detection voltage $\left(\mathrm{V}_{\mathrm{DET}}\right)$, and the VM pin voltage is in the range from overcurrent detection voltage ( $\mathrm{V}_{\mathrm{DET4} 4}$ ) to discharge overcurrent detection voltage ( $\mathrm{V}_{\mathrm{DET}}$ ). This is called the normal condition that charging and discharging can be carried out freely.

Caution: The NT1702 series may be needed connecting a charger to return to normal condition, when the battery is connected for the first time.

## (2) Overcharge Condition

1) Overcharge Protection:

When the VDD voltage is higher than the overcharge detection voltage ( $\mathrm{V}_{\mathrm{DET} 1}$ ) and lasts for longer than the overcharge detection delay time ( $\mathrm{t}_{\mathrm{VDET1}}$ ), NT1702 series turns off the external charging MOSFET to protect the pack from being overcharged, which CO pin turns to " L " from " H " level.
2) Overcharge Protection Release:
(a) When the battery voltage is lower than $V_{R E L 1}$ and the $V$ - pin voltage is between charge overcurrent detection voltage ( $\mathrm{V}_{\mathrm{DET} 4}$ ) and discharge overcurrent detection voltage ( $\mathrm{V}_{\mathrm{DET}}$ ), the NT1702 series would release this condition.
When the battery voltage is lower than $\mathrm{V}_{\mathrm{DET} 1}$ and charger is removed, the NT1702 series can be released from this condition.
(b) When the battery voltage is lower than $\mathrm{V}_{\text {REL1 }}$ and the V - pin voltage is between charge overcurrent detection voltage ( $\mathrm{V}_{\text {DET4 }}$ ) and short detection voltage ( $\mathrm{V}_{\text {SHORT }}$ ), the NT1702 series would release this condition.
When the battery voltage is lower than $\mathrm{V}_{\text {REL1 }}$ and charger is removed, the NT1702 series can be released from this condition.
*: About overcharge release condition please reference to NT1702ANO2.

## (3) Overdischarge Condition

1) Overdischarge Protection:

When the VDD voltage is lower than the overdischarge detection voltage ( $\mathrm{V}_{\mathrm{DET} 2}$ ) and lasts longer than overdischarge detection delay time ( $\mathrm{t}_{\mathrm{VDET} 2}$ ), NT1702 series turns off the external discharge MOSFET to protect the pack from being overdischarged, which DO pin turns to "L" from "H" level. In overdischarge condition V-pin is pulled-up to VDD by a resistor (RVMD) between the V- pin and VDD pin. After that, when V - pin voltage is higher than $\mathrm{VDD} / 2(\mathrm{Typ})$, the IC gets to power down mode.
2) Overdischarge Protection Release:

The overdischarge protection is released when
(a) a charger is connected and V - pin voltage is lower than -0.7 V (Typ.) and battery voltage is higher than the overdischarge voltage, or
(b) a charger is connected, and V - pin voltage is higher than -0.7 V (Typ.) and battery voltage is higher than the overdischarge release voltage.

## (4) Discharge Overcurrent Condition

1) Discharge Overcurrent Protection:

The NT1702 series provides discharge overcurrent protection and load short-circuiting protection:
(a) Discharge overcurrent protection occurs when V - pin voltage between $\mathrm{V}_{\text {DET3 }}$ and $\mathrm{V}_{\text {SHORT }}$ and lasts for a certain delay time ( $\mathrm{t}_{\mathrm{VDET}}$ ) or longer.
(b) Load short-circuiting protection occurs when V - pin voltage higher than $\mathrm{V}_{\text {SHORT }}$ and lasts for a certain delay time ( $\mathrm{t}_{\text {SHORT }}$ ) or longer.
When above conditions happen, the DO pin goes "L" from " $H$ " to turn off the discharging MOSFET.
In discharge overcurrent and load short-circuiting conditions, V- pin is pulled-down to Vss pin by the internal resistor (RVMS).
2) Discharge Overcurrent and Load Short-Circuiting Protection Release:

The IC detects the status by monitoring V-pin voltage that is inversely proportional to the impedance (Rload) between two terminals (EB+ and EB-). The Rload increases while the $V$ - pin voltage decreases. When the V - pin voltage equals to $\mathrm{V}_{\text {SHORT }}$ or lower, discharge overcurrent status returns to normal mode. The relation between V - and Rload is shown as follows:

$$
\mathrm{V}-=\frac{\mathrm{RVMS}}{\mathrm{RVMS}+\text { Rload }} \text { X VDD ; where V- } \leqq \text { Vshort }
$$

## (5) Charge Overcurrent Condition

The NT1702 series provides charge overcurrent protection to prevent the battery pack from being connected to an unexpected charger.

1) Charge Overcurrent Protection

When the voltage of V - pin is lower than charge overcurrent detection voltage ( $\mathrm{V}_{\mathrm{DET4} 4}$ ) and lasts for a certain delay time ( $\mathrm{t}_{\mathrm{DET} 4}$ ) or longer, the CO pin goes "L" from " H " to turn off the charging MOSFET.
2) Charge Overcurrent Release: Charge overcurrent protection can be only released by disconnecting the charger.

## (6) Power Down Condition

1) Entering to Power Down Mode:

NT1702 series enters the power down mode when overdischarge protection occurs and $V$ - pin voltage is higher than VDD/2 (typical). The V - pin voltage is pulled-up to the VDD through the $\mathrm{R}_{\mathrm{VmD}}$ resistor. The internal circuits is shut off, therefore, the power-down current (I $\mathrm{I}_{\text {Standby }}$ ) is reduced to be low 0.2uA (Max.).
2) Power Down Mode Release:

The power down mode is released when a charger is connected and V - pin voltage is lower than VDD/2 (typical).
Note: Power down condition is for power down mode enabled version only.

## Block Diagram



## Timing Chart

(1) Overcharge, Charge Overcurrent Operation

*: The charger is assumed to charge with a constant current.
(2) Overdischarge, Discharge Overcurrent, Load Short-Circuiting Operation


## Recommended Application Circuit



Table1 Constant for external components

| Symbol | Parts | Purpose | Recommended | Min. | Max. | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FET1 | N channel MOSFET | Discharge control | ---- | ---- | ---- | *1) $0.4 \mathrm{~V} \leq$ Threshold voltage $\leq$ Overdischarge detection voltage. Gate to source withstand voltage $\geq$ Charger voltage. |
| FET2 | N channel MOSFET | Charge control | ---- | ---- | ---- | *1) $0.4 \mathrm{~V} \leq$ Threshold voltage $\leq$ Overcharge detection voltage. Gate to source withstand voltage $\geq$ Charger voltage. |
| R1 | Resistor | ESD protection for power fluctuation | $470 \Omega$ | $240 \Omega$ | $1 \mathrm{~K} \Omega$ | *2) Set Resistance to the value 2R1< R2. |
| C1 | Capacitor | For power fluctuation | 0.1uF | 0.022uF | 1.0uF | *3) Install a 0.022 uF capacitor or higher. |
| R2 | Resistor | Protection for reverse connection of a charger | $1 \mathrm{~K} \Omega$ | $300 \Omega$ | $2 \mathrm{~K} \Omega$ | *4) The resistor is preventing big current when a charger is connected in reverse. |

[^0]*3) Applying a smaller capacitance C1 to system, DO may failed to function when load short-circuiting is detected.
*4) If R2 resistance is higher than $2 k \Omega$, the charging current may not be cut when a high-voltage charger is connected.
*5) As followed this recommended table, the system ESD level could be reached at least $\pm 12 \mathrm{KV}$.

Caution: 1) The above constants may be changed without notice.
2) The application circuit above is for reference only. To determine the correct constants, evaluation of actual application is required.

Precautions: 1) The application condition for the input voltage, output voltage, and load current should not exceed the package power dissipation.
2) Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

## Characteristics (Typical Data)

a) Current consumption

1) IDD vs. Ta.

2) Istandby vs. Ta.

3) Istandby vs. $V_{D D}$

b) Overcharge detection voltage / overdischarge detection voltage / overcurrent detection voltage, and delay time.

4) $\mathrm{t}_{\mathrm{DET} 1} \mathrm{vs}$. Ta.

5) $\mathrm{tV}_{\text {REL1 }}$ vs. Ta.

6) $V_{R E L 1}$ vs. Ta.

7) $V_{D E T 2}$ vs. Ta.


8) $\mathrm{t}_{\mathrm{DET} 2}$ vs. Ta.

9) $V_{\text {DET3 }}$ vs. Ta.

10) $\mathrm{V}_{\text {SHORT }}$ vs. Ta.

11) $\mathrm{tV}_{\mathrm{DET}} \mathrm{Vs} . \mathrm{Ta}$.


12) $\mathrm{V}_{\mathrm{DET} 4}$ Vs. Ta.

13) $\mathrm{t}_{\mathrm{DET3}}$ vs. $\mathrm{V}_{\mathrm{DD}}$

14) $t V_{D E T 4}$ vs. $V_{D D}$

15) $\mathrm{t}_{\mathrm{DET} 4}$ vs. Ta.

16) $\mathrm{V}_{\text {SHORT }}$ vs. $V_{D D}$

17) $t V_{D E T 1}$ vs. $V_{D D}$

18) $\mathrm{V}_{\mathrm{DET3}}$ vs. V - pin voltage

19) $t V_{D E T 2}$ vs. $V_{D D}$

20) $\mathrm{IV}_{\text {DET4 }}$ vs. V - pin voltage

21) $\mathrm{V}_{\text {DET3 }}$ and $\mathrm{V}_{\text {SHORT }}$ vs. V - pin voltage

c) Output resistor

22) $R_{\text {DOH }}$ vs. Ta.

23) $R_{V M S}$ vs. Ta.

24) $R_{\text {col }}$ vs. Ta.

25) $R_{\text {DOL }}$ vs. Ta.

26) $R_{\text {vMd }}$ vs. Ta .

27) $I_{\mathrm{COH}}$ vs. $\mathrm{V}_{\mathrm{CO}}$

28) $I_{C O L}$ vs. $V_{C O}$

29) $I_{D O H}$ vs. $V_{D O}$

30) $I_{D O L}$ vs. $V_{D O}$


## Marking Information

SOT-23-5
Top view


1) : Product code (A)
2) : Type code (U)
3) to 5) : Version code
4) to 9) : Lot number

SOT-23-6
Top view


1) : Product code (A)
2) $\quad:$ Type code (U)
3) to 5) : Version code
4) to 9) : Lot number

DFN-6L

1) : Product code (A)
2) : Type code (U)
3) to 4) : Version code
4) to 8) : Lot numbe


Product name vs. Version code

| Product name | Version code |  |  |
| :---: | :---: | :---: | :---: |
|  | SOT-23-5 | SOT-23-6 | DFN-6L |
|  | 3) 4) 5) | 3) 4) 5) | 3) 4) |
| NT1702-HFK | HFK | HFK | 02 |
| NT1702-HQM | - | HQM | 03 |
| NT1702-HQR | HQR | HQR | 04 |
| NT1702-HFR | HFR | - | 05 |
| NT1702-FLK | - | FLK | 06 |
| NT1702-HXW | HXW | - | 07 |
| NT1702-GZK | - | GZK | - |
| NT1702-JQM | JQM | - | $0 C$ |

## Package Information

SOT-23-5 Dimensions


| SYMBOL | MIN | NOM | MAX |
| :---: | :---: | :---: | :---: |
| A | - | - | 1.45 |
| A1 | 0.00 | - | 0.15 |
| A2 | 0.90 | 1.15 | 1.30 |
| b | 0.30 | 0.4 | 0.50 |
| c | 0.08 | - | 0.22 |
| D | 2.70 | 2.90 | 3.10 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.40 | 1.60 | 1.80 |
| e | - | 0.95 BSC | - |
| e1 | - | 1.90 BSC | - |
| L | 0.30 | 0.45 | 0.60 |
| L1 | - | 0.6 REF | - |
| L2 | - | 0.25 BSC | - |
| $\theta$ | $0^{\circ}$ | 4 | $8^{\circ}$ |
| $\theta$ 1 | $5^{\circ}$ | $10^{\circ}$ | $15^{\circ}$ |

## SOT-23-6 Dimensions



| SYMBOL | MIN | NOM | MAX |
| :---: | :---: | :---: | :---: |
| A | - | - | 1.45 |
| A1 | 0.00 | - | 0.15 |
| A2 | 0.90 | 1.15 | 1.30 |
| b | 0.30 | 0.4 | 0.50 |
| c | 0.08 | - | 0.22 |
| D | 2.70 | 2.90 | 3.10 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.40 | 1.60 | 1.80 |
| e | - | 0.95 BSC | - |
| e1 | - | 1.90 BSC | - |
| L | 0.30 | 0.45 | 0.60 |
| L1 | - | 0.6 REF | - |
| L2 | - | 0.25 BSC | - |
| $\theta$ | $0^{\circ}$ | $4^{\circ}$ | $8^{\circ}$ |
| $\theta$ 1 | $5^{\circ}$ | $10^{\circ}$ | $15^{\circ}$ |

DFN-6L Dimension

B


TDP VIEW


1. DDENS[DN AND TDERANCING CDNFDRM TD ASNE Y14.5M-1994.
2. CDNTRLLLNG DLNENSIDNS , M] LLMETER, CDNVERTED [NCH dJensam are nat mecessaelly exact.

| Symbol | Dimensions In <br> Millimeters |  |
| :---: | :---: | :---: |
|  | Min. | Max. |
| A | 0.350 | 0.550 |
| A1 | 0.000 | 0.050 |
| A3 | 0.127 REF |  |
| D | 1.424 | 1.620 |
| E | 1.924 | 2.150 |
| D2 | 1.000 | 1.200 |
| E2 | 0.800 | 1.000 |
| b | 0.150 | 0.300 |
| e | 0.500 | BSC |
| L | 0.174 | 0.370 |


[^0]:    *1) If the threshold voltage of an FET is lower than 0.4 V , the FET may failed to stop the charging current.
    If an FET has a threshold voltage equal to or higher than the overdischarge detection voltage, discharging may be stopped before overdischarge is detected.
    If the charger voltage is higher than the withstanding voltage between the gate and source, the FET may be damaged.
    *2) Employing an over-specification (listed in above table) R1 may result in overcharge detection voltage and release voltage higher than the defined voltage (listed in page 4)
    If R1 has a higher resistance, the IC may be damaged caused by over absolute maximum rating of VDD voltage when a charger is connected reversely.

